CLAIMS

1. A current source comprising:

first means for generating a current in response to an applied voltage and a resistance variable in response to a control signal, and

second means for supplying said control signal.

2. The invention of Claim 1 wherein said first means includes a resistive network comprising a first plurality of resistors R_a, R_b, ..., R_m.

3. The invention of Claim 2 wherein said first plurality of resistors R_a, R_b, ..., R_m are connected in parallel across a first node A and a second node B.

4. The invention of Claim 3 wherein said resistive network further includes a first plurality of switches S_1, S_2, ...S_m, each switch coupled to one of said first plurality of resistors R_a, R_b, ..., R_m and adapted to switch said resistor in and out of said resistive network in response to said control signal.

5. The invention of Claim 4 wherein said control signal is a digital word comprised of m bits.

6. The invention of Claim 5 wherein each bit of said control signal controls one of said switches S_1, S_2, ...S_m.

7. The invention of Claim 3 wherein said first plurality of resistors R_a, R_b, ..., R_m are binarily weighted.

8. The invention of Claim 3 wherein said resistive network further includes a resistor R2 connected between node A and node B.

9. The invention of Claim 3 wherein said resistive network further includes two resistors R_A and R_B connected in series between node A and node B.

10. The invention of Claim 9 wherein said resistive network further includes a second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk}.

11. The invention of Claim 10 wherein said second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk} are connected in parallel across resistor R_B.

12. The invention of Claim 11 wherein said resistive network further includes a second plurality of switches S_{B1}, S_{B2}, ...S_{Bk}, each switch coupled to one of said second plurality of resistors R_{B1}, R_{B2}, ..., R_{Bk} and adapted to switch said resistor in and out of said resistive network in response to said control signal.

13. The invention of Claim 3 wherein said resistive network further includes a third plurality of resistors R_A, R_B, ...R_L connected in series between node A and node B.

14. The invention of Claim 13 wherein said resistive network further includes one or more resistor banks, each resistor bank including a number of resistors R_{B1}, R_{B2}, ..., R_{Bk}.

15. The invention of Claim 14 wherein said resistor banks are each connected in parallel across one or more of said third plurality of resistors R_A, R_B, ...R_L.

16. The invention of Claim 15 wherein said resistors R_{B1}, R_{B2}, ..., R_{Bk} of said resistor banks are connected in parallel.

17. The invention of Claim 16 wherein each of said resistor banks further

includes a number of switches S_{B1}, S_{B2}, ...S_{Bk}, each switch coupled to one of said resistors R_{B1}, R_{B2}, ..., R_{Bk} and adapted to switch said resistor in and out of said resistive network in response to said control signal.

18. The invention of Claim 4 wherein said switches are implemented using transistors.

19. The invention of Claim 18 wherein said switches are implemented using NMOS transistors.

20. The invention of Claim 18 wherein the number of transistors used to implement each switch is determined by the weight of the resistor that the switch is coupled to.

21. The invention of Claim 18 wherein said switches are controlled by control signals applied to the gates of said transistors.

22. The invention of Claim 2 wherein said first means further includes a transistor Q adapted to apply a voltage across said resistive network to generate a current I.

23. The invention of Claim 22 wherein a reference voltage V_{REF} is applied to the base of said transistor Q.

24. The invention of Claim 22 wherein said current I is output from the collector of said transistor Q.

25. The invention of Claim 22 wherein a first end of a resistor R1 is coupled to the emitter of said transistor Q.

26. The invention of Claim 25 wherein said node A of said resistive network is connected to a second end of said resistor R1.

27. The invention of Claim 26 wherein a first end of a resistor R3 is connected to node B of said resistive network.

28. The invention of Claim 27 wherein a second end of said resistor R3 is connected ground.

29. A current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistive network coupled to the emitter of said transistor Q, said resistive network including a plurality of resistors R_a, R_b, ..., R_m;

a circuit for supplying a digital control signal; and

a plurality of switches S_1, S_2, ...S_m, each switch coupled to one of said plurality of resistors R_a, R_b, ..., R_m and adapted to selectively switch said resistor in and out of said resistive network in response to said control signal.

30. A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current steering cells, each cell including:

a current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistive network coupled to the emitter of said transistor Q, said resistive network including a first plurality of resistors R_a, R_b, ..., R_m;

a circuit for supplying a digital control signal; and

a first plurality of switches S_1, S_2, ...S_m, each switch coupled to one of said

first plurality of resistors R_a, R_b, ..., R_m and adapted to selectively switch said resistor in and out of said resistive network in response to said control signal; and

a pair of transistors for selectively switching current from said current source between said first current summing bus and said second current summing bus in response to an input signal.

31. A current source comprising:

two resistors R1 and R3 connected in series;

first means for applying a voltage across said resistors R1 and R3 to generate a current I;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

second means for supplying said control signal.

32. The invention of Claim 31 wherein said DAC is a voltage output DAC adapted to change the voltage at said node between R1 and R3.

33. The invention of Claim 31 wherein said DAC is a current output DAC adapted to add a current at said node between R1 and R3.

34. The invention of Claim 31 wherein said first means includes a transistor Q.

35. The invention of Claim 34 wherein a reference voltage V_{REF} is applied to the base of said transistor Q.

36. The invention of Claim 34 wherein said current I is output from the collector of said transistor Q.

37. The invention of Claim 34 wherein said resistor R1 is coupled to the emitter

of said transistor Q.

38. The invention of Claim 34 wherein said resistor R3 is connected ground.

39. A current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistor R1 connected to the emitter of transistor Q;

a resistor R3 having one end connected in series to R1 and the other end connected to ground;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

a circuit for supplying said control signal.

40. A digital to analog converter comprising:

a first current summing bus;

a second current summing bus; and

a plurality of current steering cells, each cell including:

a current source comprising:

a transistor Q adapted to receive a voltage V_{REF} at its base and output a current I at its collector;

a resistor R1 connected to the emitter of transistor Q;

a resistor R3 having one end connected in series to R1 and the other end connected to ground;

a digital to analog converter (DAC) adapted to apply a voltage or current at the node between said resistors R1 and R3 to change the current I in response to a control signal input to said DAC; and

a circuit for supplying said control signal; and

a pair of transistors for selectively switching current from said current

source between said first current summing bus and said second current summing bus in response to an input signal.

41. A method for trimming a current source including the steps of:

creating a resistive network comprised of a plurality of resistors;

applying a voltage across said resistive network to generate a current I; and

selectively switching said resistors in and out of said resistive network until said current I is at a desired value.

42. A method for trimming a current source including the steps of:

connecting two resistors R1 and R3 in series;

applying a first voltage across said resistors R1 and R3 to generate a current I; and

connecting the output of a digital to analog converter to the node between R1 and R3;

changing the digital input to said digital to analog converter until said current I is at a desired value.